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APPLICATION NO.	APPLICATION NO. FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/733,038 12/11/2003		12/11/2003	Theodore W. Houston	TI-35881	8454		
23494	7590	04/14/2006		EXAM	EXAMINER		
		ENTS INCORPOR	LE, THONG QUOC				
P O BOX 65 DALLAS, 7	•		ART UNIT	PAPER NUMBER			
· ·				2827			
				DATE MAILED: 04/14/2006			

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application !	lo.	Applicant(s)		m			
		10/733,038		HOUSTON, THEODORE W.		(
	Office Action Summary	Examiner		Art Unit					
		Thong Q. Le		2827					
Period fo	The MAILING DATE of this communi	cation appears on the co	ver sheet with the c	orrespondence ad	ldress				
A SHO WHIC - Exter after - If NO - Failui Any r	ORTENED STATUTORY PERIOD FOR THE MANAGEMENT OF T	AILING DATE OF THIS of 37 CFR 1.136(a). In no event, I unication. Intory period will apply and will ex will, by statute, cause the application.	COMMUNICATION nowever, may a reply be timpire SIX (6) MONTHS from to become ABANDONEI	l. ely filed the mailing date of this co D (35 U.S.C. § 133).					
Status									
1)⊠	Responsive to communication(s) file	d on 17 January 2006.							
•	This action is FINAL . 2b)⊠ This action is non-final.								
, —	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims								
4) 又	Claim(s) 1-10 and 12-21 is/are pendi	ng in the application.							
	4a) Of the above claim(s) is/are withdrawn from consideration.								
	Claim(s) is/are allowed.								
,	Claim(s) <u>1-5,9,10,12-16,20 and 21</u> is/are rejected.								
	Claim(s) <u>6-8 and 17-19</u> is/are objected to.								
	Claim(s) are subject to restrict		iirement.						
Applicati	ion Papers								
9)□	The specification is objected to by the	Examiner.							
	The drawing(s) filed on is/are:		objected to by the I	Examiner.					
. • / 🗀	Applicant may not request that any object								
	Replacement drawing sheet(s) including				FR 1.121(d).	•			
11)	The oath or declaration is objected to								
Priority u	ınder 35 U.S.C. § 119								
12)	Acknowledgment is made of a claim t ☐ All b)☐ Some * c)☐ None of:	for foreign priority under	35 U.S.C. § 119(a))-(d) or (f).					
	1. Certified copies of the priority								
	2. Certified copies of the priority								
	3. Copies of the certified copies	of the priority document	s have been receive	ed in this National	Stage				
	application from the Internation								
* 5	See the attached detailed Office action	n for a list of the certified	d copies not receive	ed.					
Attachmen	·			(DTO 446)					
	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (P	4) TO-948)	Interview Summary Paper No(s)/Mail D						
3) 🔲 Infor	mation Disclosure Statement(s) (PTO-1449 or er No(s)/Mail Date	PTO/SB/08) 5)		Patent Application (PT	O-152)				

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DETAILED ACTION

- 1. Amendment filed on 01/17/2006 has been entered.
- 2. Claims 1-10, 12-21 are presented for examination.

Response to Arguments

3. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claims 1-5,9-10,12-16,20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wendell (U.S. Patent No. 5,936,892).

Regarding claims 1, 12, Wendell discloses an SRAM device (Figure 1) comprising:

an SRAM array (Figure 1, 10) coupled to row peripheral circuitry (Figure 1, 16) by word line (Figure 1, WL) and coupled to column peripheral circuitry (Column 22, lines 55-58, column decoder) by bit lines (Figure 1, BLT, BLC); and

an array low voltage control circuitry (Figure 1, 28) that provides an enhanced low operating voltage Vess to SRAM array during at least a portion of an active mode

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thereof, (Column 4, lines 54-65) the enhanced low operating voltage Vess having a higher value than a low operating voltage Vss (Column 5, lines 10-27).

Regarding claims 2, 13, Wendell discloses wherein the array low voltage control circuitry provides the enhanced low operating voltage Vess only during a write operation (Column 4, lines 55-56).

Regarding claims 3, 14, Wendell discloses wherein the array low voltage control circuitry provides the enhanced low operating voltage Vess only during all of active mode (Column 4, lines 55-56, read and write mode).

Regarding claims 4, 15, Wendell discloses wherein the array low voltage control circuitry provides the enhanced low operating voltage Vess only during all modes (Column 5, lines 3-6).

Regarding claims 5, 10, 16, 21, Wendell discloses wherein the array low voltage control circuitry provides the enhanced low operating voltage Vess based on a factor selected from the group consisting of a transistor parameter (Figure 1, 36,34).

Regarding claims 9,20 Wendell discloses wherein the array low voltage control circuitry employs an active component to provide the enhance low operating voltage Vess (Column 4, lines 65-67,Column 5, lines 1-3).

Allowable Subject Matter

6. Claims 6-8, 17-19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Claims 6-8 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. wendell (U.S. Patent No. 5,936,892), and others, does not teach the claimed invention having wherein the array low voltage control circuitry provides the enhanced low operating voltage Vess at higher value when based on a strong n process corner as claims 6, 17 disclosed, and Vess lower value during a read operation than during a write operation as claims 7, 18 disclosed, and the array low voltage control circuitry only provides the lower value for an addressed column of the SRAM as claims 8, 19 disclosed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Business Center (EBC) at 866-217-9197 (toll-free).

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Thong Q. Le

Primary Examiner

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4/7/2006